CLAIMS

We claim:

1. A programmable device having programmable input/output (I/O) circuitry and programmable logic connected to receive incoming signals from and provide outgoing signals to the I/O circuitry, wherein:

the I/O circuitry can be programmed to function in an independent mode of operation in which first and second pads of the programmable device operate independent of one another; and

the I/O circuitry can be programmed to function in one or more dependent modes of operation in which a pair of related signals appear at the first and second pads, respectively.

2. The invention of claim 1, wherein the programmable device is an FPGA.

3. The invention of claim 1, wherein, for the first and second pads, the I/O circuitry comprises:

(a) a first programmable impedance (e.g., RT1 of Fig. 2) switchably (e.g., ST1) connected between the first pad (e.g., pad T) and a first terminal (e.g., VT1);

(b) a second programmable impedance (e.g., RT2) switchably (e.g., ST2) connected between the first pad (e.g., pad T) and a second terminal (e.g., VT2);

(c) a third programmable impedance (e.g., RC1) switchably (e.g., SC1) connected between the second pad (e.g., pad C) and a third terminal (e.g., VC1);

(d) a fourth programmable impedance (e.g., RC2) switchably (e.g., SC2) connected between the second pad (e.g., pad C) and a fourth terminal (e.g., VC2); and

(e) a fifth programmable impedance (e.g., RDT, RDC) switchably (e.g., SDT, SDC) connected between the first pad (e.g., pad T) and the second pad (e.g., pad C).

4. The invention of claim 3, wherein each programmable impedance is a programmable resistor.

5. The invention of claim 3, wherein each programmable impedance is independently programmable.

6. The invention of claim 3, wherein a third pad (e.g., pad P) of the programmable device is switchably (e.g., SC) connected to a node (e.g., VCM) along the switchable connection between the first and second pads.

7. The invention of claim 6, wherein:

a first part (e.g., RDT) of the fifth programmable impedance is switchably (e.g., SDT) connected to the node (e.g., VCM); and

a second part (e.g., RDC) of the fifth programmable impedance is switchably (e.g., SDC) connected to the node (e.g., VCM).

8. The invention of claim 3, wherein:

the first programmable impedance (e.g., RT1) and the second programmable impedance (e.g., RT2) can be programmably operated as a first push-pull buffer; and

the third programmable impedance (e.g., RC1) and the fourth programmable impedance (e.g., RC2) can be programmably operated as a second push-pull buffer.

9. The invention of claim 8, wherein:

the first push-pull buffer is implemented as a combination of two or more smaller programmable push-pull buffers (e.g., BT1-BT3 of Fig. 8); and

the second push-pull buffer is implemented as a combination of two or more smaller programmable push-pull buffers (e.g., BC1-BC3).

10. The invention of claim 3, wherein reference voltages or data signals can be independently applied to each terminal.

11. The invention of claim 1, wherein the one or more dependent modes of operation include both differential and complementary modes of operation.

12. The invention of claim 1, wherein the one or more dependent modes of operation include both signal-driving and signal-receiving modes of operation.

13. The invention of claim 1, wherein the one or more dependent modes of operation include both symmetric and non-symmetric modes of operation.

14. The invention of claim 1, wherein the one or more dependent modes of operation comprise one or more differential modes of operation in which a pair of differential signals appear at the first and second pads, respectively.

15. The invention of claim 14, wherein the I/O circuitry supports a plurality of different differential modes of operation having different combinations of high, low, common mode, and differential voltage levels.

16. The invention of claim 1, wherein the one or more dependent modes of operation comprise one or more complementary modes of operation in which a pair of complementary signals appear at the first and second pads, respectively.

17. The invention of claim 16, wherein the I/O circuitry supports a plurality of different complementary modes of operation having different combinations of high, low, common mode, and differential voltage levels.

18. The invention of claim 1, wherein the one or more dependent modes of operation include both differential and complementary modes of operation, both signal-driving and signal-receiving modes of operation, and both symmetric and non-symmetric modes of operation.

19. The invention of claim 1, wherein:

the programmable device is an FPGA;

for the first and second pads, the I/O circuitry comprises:

(a) a first programmable resistor (e.g., RT1 of Fig. 2) switchably (e.g., ST1) connected between the first pad (e.g., pad T) and a first terminal (e.g., VT1);

(b) a second programmable resistor (e.g., RT2) switchably (e.g., ST2) connected between the first pad (e.g., pad T) and a second terminal (e.g., VT2);

(c) a third programmable resistor (e.g., RC1) switchably (e.g., SC1) connected between the second pad (e.g., pad C) and a third terminal (e.g., VC1);

(d) a fourth programmable resistor (e.g., RC2) switchably (e.g., SC2) connected between the second pad (e.g., pad C) and a fourth terminal (e.g., VC2); and

(e) a fifth programmable resistor (e.g., RDT, RDC) switchably (e.g., SDT, SDC) connected between the first pad (e.g., pad T) and the second pad (e.g., pad C);

each programmable resistor is independently programmable;

a third pad (e.g., pad P) of the programmable device is switchably (e.g., SC) connected to a node (e.g., VCM) along the switchable connection between the first and second pads;

a first part (e.g., RDT) of the fifth programmable resistor is switchably (e.g., SDT) connected to the node (e.g., VCM);

a second part (e.g., RDC) of the fifth programmable resistor is switchably (e.g., SDC) connected to the node (e.g., VCM);

the first programmable resistor (e.g., RT1) and the second programmable resistor (e.g., RT2) can be programmably operated as a first push-pull buffer;

the third programmable resistor (e.g., RC1) and the fourth programmable resistor (e.g., RC2) can be programmably operated as a second push-pull buffer;

the first push-pull buffer is implemented as a combination of two or more smaller programmable push-pull buffers (e.g., BT1-BT3 of Fig. 8);

the second push-pull buffer is implemented as a combination of two or more smaller programmable push-pull buffers (e.g., BC1-BC3);

reference voltages or data signals can be independently applied to each terminal; and

the one or more dependent modes of operation include both differential and complementary modes of operation, both signal-driving and signal-receiving modes of operation, and both symmetric and non-symmetric modes of operation, wherein the one or more dependent modes of operation comprise:

one or more differential modes of operation in which a pair of differential signals appear at the first and second pads, respectively, wherein the I/O circuitry supports a plurality of different differential modes of operation having different combinations of high, low, common mode, and differential voltage levels; and

one or more complementary modes of operation in which a pair of complementary signals appear at the first and second pads, respectively, wherein the I/O circuitry supports a plurality of different complementary modes of operation having different combinations of high, low, common mode, and differential voltage levels.

20. A programmable termination circuit integrated within a programmable device and adapted to provide programmable, resistive interconnections between input/output (I/O) pads of the programmable device, the termination circuit comprising:

a plurality of programmable resistors;

a plurality of programmable switches connecting the programmable resistors; and

a plurality of voltage terminals connected to at least some of the programmable resistors and adapted to receive one or more a programmable reference voltages.

21. A method for operating a programmable device, comprising:

programming I/O circuitry of the programmable device to function in an independent mode of operation in which first and second pads of the programmable device operate independent of one another; and

programming the I/O circuitry to function in a dependent mode of operation in which a pair of related signals appear at the first and second pads, respectively.